REMARKS

Filed concurrently herewith is a request for a two month extension of time which extends the shortened statutory period for response to September 6, 2005. Accordingly, Applicant respectfully submits that this response is being timely filed.

The Official Action dated April 6, 2005 has been received and its contents carefully noted. In view thereof, claims 1-7 have been canceled in favor of new claims 9-16 in order to better define that which Applicant regards as the invention. Accordingly, claims 9-16 are presently pending in the instant application.

With reference now to the Official Action and particularly page 2 thereof, claims 1-5 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 3,083,907 issued to Crocker et al. This rejection is respectfully traversed in that the patent to Crocker et al. neither discloses nor remotely suggests that which is presently set forth by Applicant's claimed invention.

Initially, Applicant wishes to acknowledge the Examiner's indication in the Office Action Summary Page that claim 8 is allowable over the prior art of record. It is respectfully requested that claim 8, again, be indicated as being allowable along with new claims 9-16 set forth hereinabove.

In rejecting Applicant's claimed invention, the Examiner states that Crocker et al. discloses in Figs. 1 and 2, a circuit comprising an input means, a pulse generating means, a plurality of modules including a first control means having a first detection means and means for generating the first reset signal and a second control means having a second detection means and means for generating a second reset signal, all connected and operating similarly as recited by Applicant. Insofar as this rejection applies to new independent claim 9, it is respectfully submitted that independent claim 9 recites a reset circuit embedded in a large

scale integrated circuit comprising an input terminal which receives a reset signal of the large scale integrated circuit from the outside, the pulse generating circuit connected to the input terminal, which generates a reset pulse signal by performing a logical operation with the reset signal, a first module connected to the pulse generation circuit wherein the first module comprises a first register connected to the pulse generation circuit which is reset in response to the reset pulse signal and a first control circuit connected to the pulse generation circuit which generates a first module reset signal by performing a logical operation with the reset pulse signal and a second module connected to the pulse generation circuit and the first module and the first module wherein the second module comprises a second register connected to the first control circuit of the first module which is reset in response to the first module reset signal and a second control circuit connected to the pulse generation circuit which generates a second module reset signal by performing a logical operation with the reset pulse signal. Clearly, these features are neither disclosed in nor suggested by the patent to Crocker et al.

Specifically, as the Examiner can readily appreciate, the present invention as recited in independent claim 9 includes a second module connected to the pulse generation circuit and the first module wherein the second module comprises a second register connected to the first control circuit of the first module which is reset in response to the first module reset signal and a second control circuit connected to the pulse generation circuit which generates a second module reset signal by performing a logical operation with the reset pulse signal. However, Crocker et al. merely shows the counting elements A-G, with each of the elements A-G being connected to an individual gating circuit 15. Specifically, Crocker et al. fails to show that the elements A-G are connected to a common gating circuit as is recited by Applicant's claimed invention. Accordingly, it is respectfully submitted that Applicant's

claimed invention as set forth in independent claim 9 as well as those claims which depend therefrom clearly distinguishes over the teachings of Crocker et al. and are in proper condition for allowance.

Further on page 2 of the Office Action, claims 6 and 7 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,164,970 issued to Shin et al. This rejection is likewise respectfully traversed in that the patent to Shin et al. neither discloses nor suggests that which is presently set forth by Applicant's claimed invention. As can be seen from the foregoing amendments, claim 6 and 7 have been canceled in their entirety. Consequently, further discussion with respect to the merits of the rejection insofar as claims 6 and 7 are concerned is no longer believed to be warranted. However, insofar as this rejection applies to new claims 14-16, Applicant provides the following.

In rejecting independent claim 6, the Examiner states that Shin et al. discloses in Fig. 1A a circuit comprising a reset input means, a clock input means, a clock control means, a plurality of modules and a plurality of delay means are connected in operating similarly to that set forth by Applicant's claimed invention. In this regard, new independent claim 14 recites a reset circuit embedded in a large scale integrated circuit comprising an input terminal which receives a reset signal having first and second potential levels, a clock terminal which receives a clock signal, a control circuit connected to the input terminal which generates a signal having the second potential level when the reset signal having the second potential level is input until a second delay reset signal is input, a first delay circuit connected to the control circuit and the clock terminal which generates a first delay reset signal using the input control from the control circuit in synchronization with the clock signal, a second delay circuit connected to the first delay circuit and the clock terminal, which generates a second delay reset signal using the first delay reset signal in synchronization with the clock

signal, a first module connected to the first delay circuit wherein the first module comprises a first register circuit which is initialized by synchronization with the clock signal and the first delay reset signal and a second module connected to the second delay circuit, wherein the second module comprises a second register circuit which initialized in synchronization with the clock signal and the second delay reset signal. Clearly, the patent to Shin et al. fails to disclose such features.

Specifically, as the Examiner can readily appreciate, independent claim 14 includes a control circuit connected to the input terminal which generates a signal having the second potential level when the reset signal having the second potential level is input until a second delay reset signal is input, a second delay circuit connected to the first delay circuit and the clock terminal, which generates a second delay reset signal using the first delay reset signal in synchronization with the clock signal. In this regard, Shin et al. merely shows the flip flop 20 in the shift register 5 connected to the flip flop 30 in the data latching circuit 1. However, the input of a flip flop 20 and the shift register is not provided to the clock control circuit 3. While Shin et al. shows the flip flop 21 in the shift register 5 as being connected to the clock control circuit, the output of the flip flop 21 in the shift register 5 is not provided to any flip flop in the data latching circuit 1 and consequently, the patent to Shin et al. clearly fails to disclose or remotely suggest that which is presently set forth by Applicant's claimed invention. Accordingly, it is respectfully submitted that independent claim 14 as well as those claims which depend therefrom clearly distinguish over the teachings of Shin et al. and are in proper condition for allowance.

Therefore, in view of the foregoing it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 9-16 be indicated as

being allowable along with independent claim 8 which has been previously indicated as being allowable over the prior art of record and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,

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